Piezo • Nano • Positioning

Interfacing Fast Nanopositioners to Track-Following Servos

Leveraging the power of PI's unique Fast/Precise Dual Interface for head test

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Background

Sub-nanometer precision and accuracy plus high positioning bandwidth have made piezo nanopositioners essential for track profiling applications in spin-stand applications. However, (1) relentlessly advancing areal density requirements and (2) the advent of patterned media raise new issues for spin-stand integrators. These emerging needs require that the nanopositioner perform within the spin-stand's track-following servo loop, requiring extremely responsive positioning with highly deterministic real-time communications.

A nanopositioning system's positioning bandwidth is the combined performance of all system elements:

- The nanopositioner itself, with its characteristic resonant frequency and integrated position sensor,
- The load on the nanopositioner, which contributes mass and resonant behavior of its own, and
- The nanopositioner's controller, with potential bottlenecks in its amplifier, sensor, control loop and communications interface.

Off-the-shelf closed-loop nanopositioners such as PI's P-753 Linear Integrated Stage/Actuator offer resonant frequencies up to 5.6kHz, and custom stages PI has delivered target F_{res} of 10kHz. Meanwhile, PI's latest-generation controllers have servo update rates of 50kHz, and amplifier bandwidths in the tens of kHz. These specifications, by themselves, would seem promising for track-following applications. But nanopositioning controls and sensor designs are optimized for sub-nm-scale accuracies and stabilities, so nanopositioning servos offer system bandwidths on the order of 1kHz, which is insufficient for track-following purposes. In addition, conventional interfaces such as RS-232, USB, IEEE-488, PCI, Ethernet and even most proprietary parallel interfaces lack the responsiveness and timing determinacy needed for integration into external tracking servos. Furthermore, the economics of production head-test demand that point-to-point position settling be as quick as possible, meaning any resonant reaction of the assembly or load—down to a sub-nanometer level—must be eliminated even if unobservable to the stage's internal position sensor.

A new architecture

These emerging requirements, raised to us by a spectrum of disk-industry customers, necessitated a blank-page approach to nanopositioning system design. The result is the E-712 NanoAutomation® controller family, a next-generation platform embodying a host of revolutionary[1] technologies.

Figure 1. E-712 incorporates a high-power amplifier, a DSP-based servo CPU, 7th-order sensor conditioning, a patent-pending fast/precise parallel interface with up to 2µsec/command positioning throughput, and feedforward capability for integration into external tracking servos.

E-712's features include:

- A modular design featuring a leading-edge backplane that supports a wide range of standard and custom modules;
- An ultra-high-power, short- and open-proof 40W LVPZT amplifier with blistering 40kHz bandwidth;
- A DSP-based servo CPU which integrates:
  - Fast capacitive-sensor signal processing;
  - Programmable analog and digital notch filters which allow the integration engineer to desensitize the servo to observable resonances in the stage and load, facilitating higher-gain digital PID servo settings for faster motions;
  - Integrated Input Shaping® for nullification of recoil-driven resonances in stage, fixturing, load and adjacent componentry[2];
  - 7th order auto-calibration linearization (4th order for the capacitive sensor on top of 3rd order for the analog sections of the electronics) for unmatched accuracy, with static and dynamic calibration parameters stored in the motion device for convenient OEM integration.

[1] Incorporates mechanisms and algorithms protected by patents issued, applied-for or pending.

[2] Input Shaping® is a trademark of Convolve, Inc., for its patented throughput-enhancing vibration cancellation technologies. http://www.Convolve.com

Importantly, E-712 features a patent-pending bi-directional communications interface which provides highly deterministic communications with up to 2µsec motion-command throughput with feedforward capability for integration into external tracking servos.

Together, this new architecture provides ~msec closed-loop step-and-settle capability with sub-nanometer accuracies with feedforward responsiveness in the microsecond regime for integration into track-following external servo loops.

The Fast/Precise Interface with Feedforward Capability

Track-profiling is a universal production test for read-write heads. Yield issues mean virtually every head must be tested. The head is placed in a fixture on the nanopositioning stage above a spinning disk, and its write element lays down a track. The stage then increments in nm-accurate steps offset from the initial position, and the read element's response is collected as a function of position. As the tracks-per-inch increases, imperfections in the track's circularity grow significant. There are high-frequency random imperfections arising from non-repeatable runout of the spindle, as well as cyclic imperfections at the spin-rate and its harmonics (especially when tracks are written on a separate tool).

Inside a working disk drive[3], the head follows the track based on position servo information interlaced with the data. Similar capability is becoming necessary for head-test. It can require the nanopositioner to achieve a nm-accurate setpoint according to its internal capacitive sensor, and then dither about it under the command of the track-following servo.

Unfortunately, the high-bandwidth/low-amplitude track-following requirements fundamentally conflict with design principles for controllers optimized for accuracy and stability. Yet accuracy and stability are also required for track profiling!

For this reason, E-712's unique Fast/Precise parallel I/O (PIO) interface (Figure 2) allows the engineer to not only rapidly issue accurate conventional nanopositioning commands but also write track-following corrective commands directly to a digital-to-analog converter in the E-712.

The Fast/Precise PIO interface supports a subset of the controller's full command set, including conventional and fast feedforward position commands, position queries, and status queries. Fast feedforward commands can be commanded at a rate of <3µsec/command, providing the bandwidth necessary for the fastest conjectured track-following applications. Physically, the PIO interface has four input and four output pairs, with each pair configured per RS-422 standards for high-speed differential (line-driver) applications. Use of RS-422 methodology facilitates speed and reliability and helps accommodate convenient cable lengths.

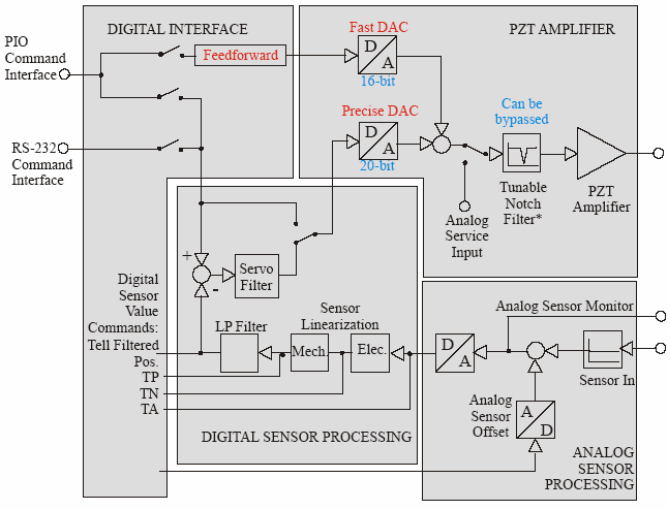

Figure 2. The patent-pending Fast/Precise interface provides feedforward functionality, facilitating fast embedded servo applications plus precise, stable conventional nanopositioning.

National Instruments' new FPGA architecture speeds PIO integration

Integration engineers may readily design their own hardware to integrate the E-712's fast/precise PIO interface. Others may wish to use commercially-available PC- or PXI-based digital I/O boards so that they might leverage the rich functionality and flexible software libraries offered by such products—especially valuable in investigatory phases of test development. However, the E-712 PIO interface's speed capabilities outstrip the capabilities of traditional digital I/O boards. An exception is National Instruments' new R-Series FPGA-based Reconfigurable I/O (RIO) devices, which are available in PCI, PXI and compact stand-alone "PAC" (Programmable Automation Controller) formats. All can integrate fast analog I/O as well. For example, PCI-7831R[4] offers 8 analog inputs at 250ksamples/sec, 8 analog outputs at 1Msample/sec, and a flexible array of 96 TTL I/O lines. This and all NI FPGA hardware is readily programmed via LabVIEW FPGA, a version of National Instruments' popular graphical programming language (Figure 3). In fact, the native parallelism of graphical programming is an ideal counterpart to the physical implementation of FPGAs since parallel loops map to separate regions of FPGA silicon and operate truly in parallel.

[3] For a brief tutorial on track servo principles, see http://www.logicsmith.com/performance.html

[4] See http://www.ni.com/pdf/products/us/04_3632_301_101.pdf

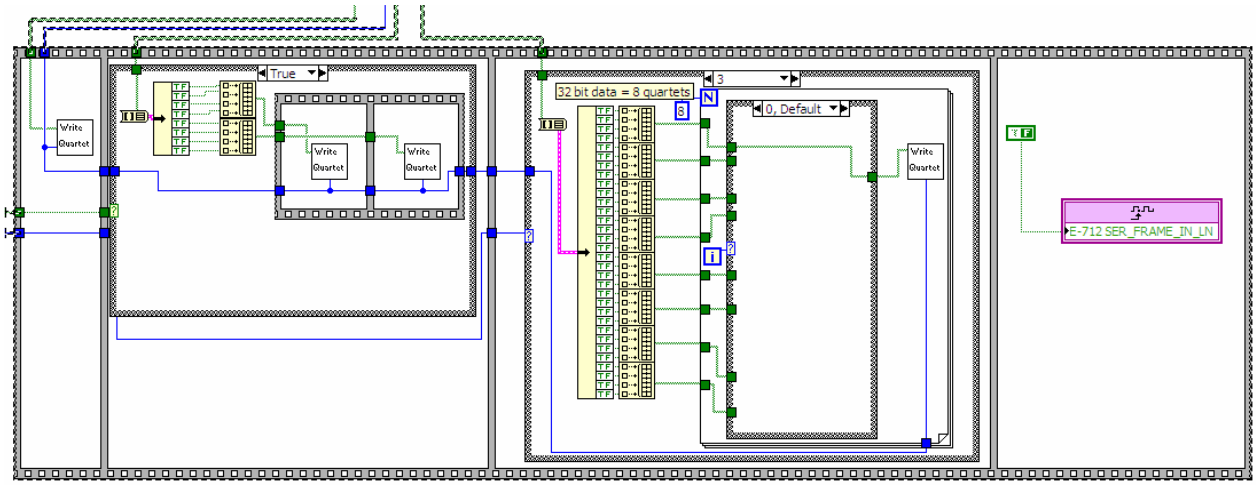

Figure 3. LabVIEW's FPGA tools allows construction of parallel, real-time operations which execute with nanosecond-scale timing. Shown is a portion of the code internal to the driver for E-712's fast PIO port. Parallel code which implements the fast tracking servo can simultaneously operate on the FPGA alongside the driver and can include additional digital and analog I/O and analysis.

The net sum is that the speed, parallelism and power of FPGAs are now accessible to anyone, and this presents a powerful platform for implementing PIO interfacing *together* with fast parallel processes such as a tracking servo (Figure 4), all running together with absolute timing determinacy.

Electrical compatibility is readily facilitated. AM26C31 and AM26C32 line drivers are recommended for level-conversion of E-712's RS-422 signals to conventional TTL levels such as that used by the NI FPGA devices. AM26LV31 and AM26LV32 provide level-conversion compatibility with LVTTL logic.

In LabVIEW, subroutines and user controls and indicators are represented as icons, and the flow of data is depicted as wires. Existing Xilinx HDL code may also be incorporated. Execution sequencing is determined by dataflow or by forced structures such as sequence frames; otherwise, functions and subroutines execute truly in parallel on the FPGA silicon. This provides a radically accessible way for engineers to devise parallel processes with high timing determinism.

The example step-and-track-follow LabVIEW FPGA sequence in Figure 4 shows a fast motion to a precise closed-loop setpoint followed by a tracking servo which commands the E-712's feedforward interface. Both execute on the FPGA. A typical track-profiling application would entail several dozen calls to this sequence, plus data acquisition and analysis. The high speed and natural parallelism of the FPGA architecture combined with the responsiveness and throughput of the E-712 architecture and the flexible power of LabVIEW programming makes it easy to investigate and deploy production-class spin-stands that incorporate tracking servos.

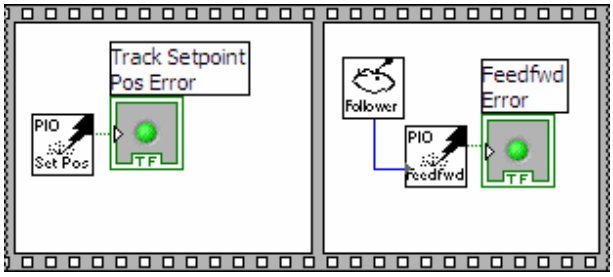

Figure 4. Example LabVIEW FPGA code for a step-and-track-follow sequence in a spinstand. Subroutines are represented by icons, with data flow represented by wires.

Results

Figure 5 below shows actual quasi-sinusoidal dither/step/dither positioning sequences made possible by the high-speed digital communications and feedforward capabilities of PI's E-712 controller when commanded by an external servo or fast command generator implemented on National Instruments' FPGA-based automation hardware using the LabVIEW FPGA programming environment.

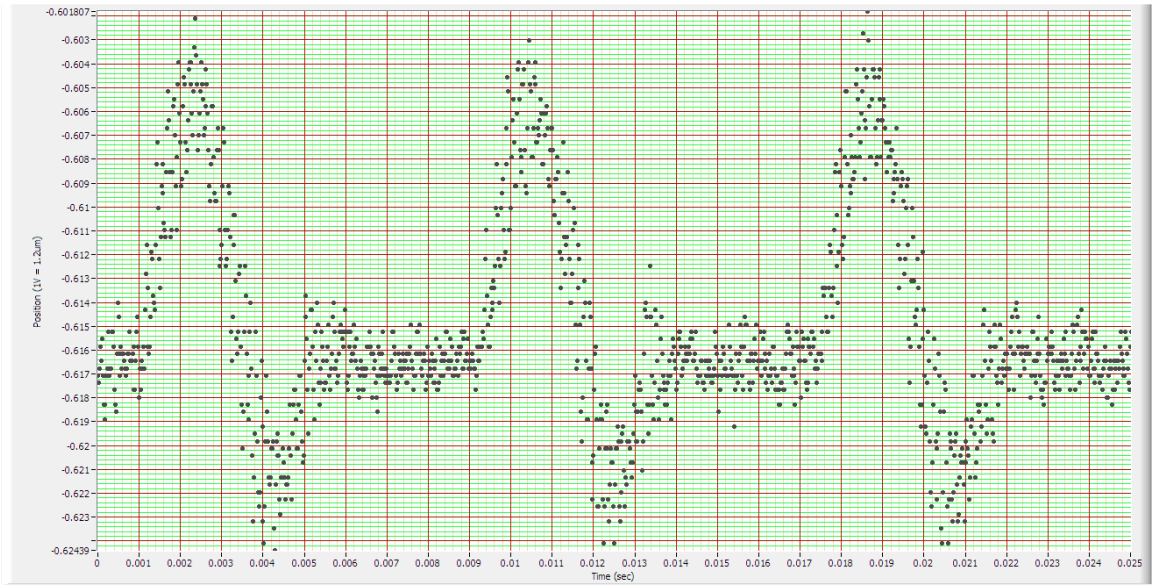

Figure 5. Simulated fast tracking sinusoid, amplitude 25nm; example shown is typical of runout compensation of a disk at 15,000 RPM under control of a track-following servo. During track profiling, nanometer-precise closed-loop increments (flat-line steps) are interleaved between the tool's sinusoidal tracking-and-data-acquisition operations; step-and-settle of these increments are complete within one revolution.

Summary

The combination of PI's E-712 controller and National Instruments' FPGA-based automation hardware and software form a powerful, flexible platform for integration engineers facing an onslaught of new head test requirements, including higher throughputs and potential production integration of track-following servos on the spin-stand.

By combining unmatched responsiveness in conventional closed-loop nanopositioning with new feedforward capability which facilitates integration into external tracking servos, E-712 helps preserve capital investments by eliminating obsolescence due to advancing production-test needs.

